Reconfigurable Threshold Logic Gates with nano-scale DG-MOSFETs

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It is expected that future nano-systems will have at its disposal a wide selection of self-assembled 'smart' materials and devices, whose fundamental properties or response may be 'tailored' as needed [1,2]. When used in conjunction with reconfigurable systems, these materials and devices will enable users to access a wide spectrum of functions without ever needing hardware change besides using on-board intelligence that issues required signals for reconfiguration. In this paper we explore short-term solutions for reconfigurable circuits using dual-gate (DG) MOSFETs that offers dynamic threshold control for individual devices [3]. Based on circuit examples simulated using TCAD and compact models, we argue that, rather than waiting for long-term material developments, reconfigurable, fault-tolerant digital systems with significant capabilities can be built using novel SOI based DG-MOSFETs devices 'just around the corner' [4]

In order to build reconfigurable logic systems, we propose a novel implementation of universal *threshold logic gates* (TLG) [5,6] based on DG-MOSFETs, which have never been proposed nor investigated before. TLG are lesser-known but more powerful logic gates that can implement not only basic Boolean gates, but also more complicated multiple-input gates such as 'minority' or 'majority' functions all by setting of an evaluation threshold *(T)* behind a summing block ($\Sigma w_i x_i$). Thus they are multi-state logic systems with a binary output. For instance, a three-input threshold gate with $w_1=w_2=w_3=1$ functions as an AND gate for T=3, an OR gate for T=1, and majority gate for T=2. Because a TLG is able to compare a user set threshold against weighted inputs ($w_i x_i$), it can also be used to build neural networks, thus having very significant application potential besides traditional logic applications.

We provide in Fig.1 the topology of a *balanced* TLG circuit built using equal number of DG-MOSFETs in both summing (Σ) and comparator block (Φ). The simulated output of a five-input TLG example with $w_1=w_2=w_3=w_4=w_5=1$ is also shown in Fig.1b for three cases of T=1, T=3 and T=5, corresponding to *OR*, *MAJORITY* and *AND* functions. A remarkable feature of this circuit is the fact that number of transistors in the summing block (Σ) is halved by use of DG-MOSFETs and the comparator block (Φ) require 2 p-MOSFETs less than conventional design [6]. Thus, the intrinsic speed advantage of DG-MOSFETs is further compounded by reduction in circuit area and power dissipation, hence leading to better performance. Moreover, it is possible to come up with an entirely new TLG design whereby both w_i and T can be easily altered at any given cycle to implement an new set of threshold functions without any hardware changes (see Fig.2). This implementation moves area savings to Φ–block while providing weight (back-bias) control for the input transistors. Therefore it is possible to implement not only a wide range of functions from a single universal TLG, but also alter the weights of threshold function $F= \Sigma w_i x_i$ at will. This would imply almost an inexhaustible list of logic functions implemented in a very compact and efficient manner.

We shall illustrate various DG-TLG topologies, and verify their correct operation, followed by a fault tolerance analysis and performance comparison with bulk counterparts. Thus, we provide valuable insight about the design of reconfigurable nano-circuits, employing novel DG-CMOS devices and unexplored topologies.

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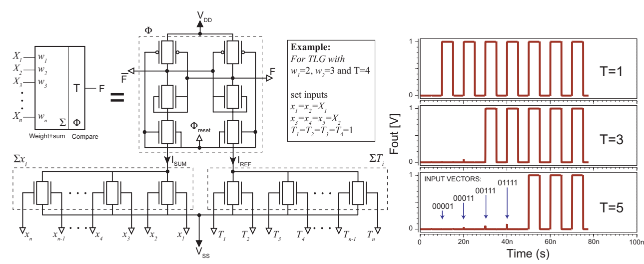

a) b)

Fig 1: (a) Generic circuit topology and (b) simulated example with n=5 for a balanced TLG example using DG-MOSFETs

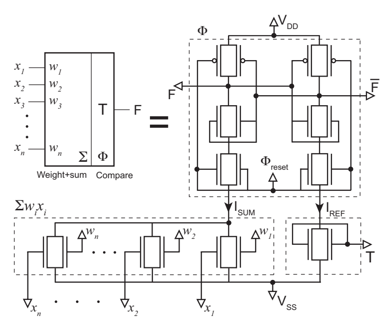

Fig 2: The proposed novel reconfigurable TLG with DG-MOSFETs. Note that for this TLG weights (w_i) in the $\sum$-block can be programmed using back-gate control of DG-MOSFET architecture

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