

Topological Implementation of Logic Functions on GaAs-based Nanowire Networks by Decision Diagram Technique

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Nanostructures and their networks are expected to play important roles in future LSI technology. One of the important issues is to utilize their topology in logic circuit realization, rather than exact size and position control. Recently, authors' group has demonstrated that utilizing binary decision diagram (BDD) logic architecture enables us to apply hexagonal nanowire networks to implementing logic circuits [1,2]. The purpose of this paper is to implement binary logic functions on GaAs-based nanowire networks with various topologies utilizing decision diagram (DD) technique, considering topological similarity between DD representation of logic function and nanowire network structures.

The decision diagram (DD) represents a logic function by a directed graph, instead of logic gates. Each node in the graph has three branches and certain nodes, called as node devices, have a function to switch output terminals for information messengers entered from root, according to a Boolean input, x_i , as shown in Fig. 1(a). Integrating node devices, any combinational logic function can be designed. Since node devices have T- or Y-configurations, grid, stretcher or hexagonal networks are suitable for their integration. Then, the DD technique makes it possible to implement logic functions on hardware topologically using nanowire networks.

For hardware implementation, GaAs-based nanowire networks controlled by Schottky wrap gate (WPG) were used. The WPG is a nanoscale Schottky gate wrapped around the nanowire. A WPG-based node device is schematically shown in Fig. 1(b). Electrons are used as messengers. Their output

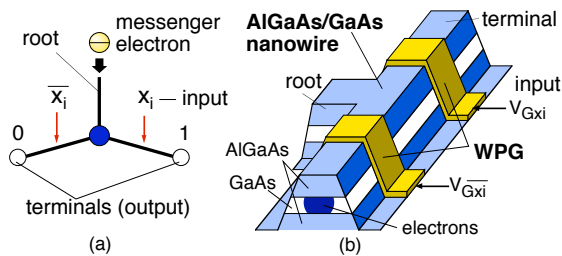


Fig. 1 (a) A DD node device and (b) its implementation by GaAs-based nanowires with Schottky WPGs.

terminals are switched by switching WPG voltages on branches for terminals in complementary fashion.

As a novel DD device, "2D hypercube"[3] was designed and fabricated, where three T-shaped node devices are embedded compactly in a 2D hypercube topology. Figure 2(a) shows a SEM image of the fabricated device with its architecture-level design. Nanowires with 600 nm width were formed by EB lithography and etching of an AlGaAs/GaAs heterostructure. The device was successfully realized utilizing a grid-like GaAs-based nanowire network controlled by WPGs, with area of $2.5 \mu\text{m} \times 3.5 \mu\text{m}$.

Measured input-output waveforms are shown in Fig. 2(b). In the measurement, messenger electrons were sent from the root to four terminals and they were detected at each terminal as output current. Input signals, x_0 and x_1 , were given as WPG voltages. A correct operation was successfully obtained at room temperature as shown in Fig. 2(b). Difference of current levels was caused by a narrow wiring on the root. The fabricated device has multifunction, for example, terminals (11) and (10)+(01) give AND and exclusive OR, respectively, then the device can operate as a full adder. The obtained result indicates the possibility of compact implementation of complex logic functions by small regular arrays of hypercube having a 2D cubic lattice topology.

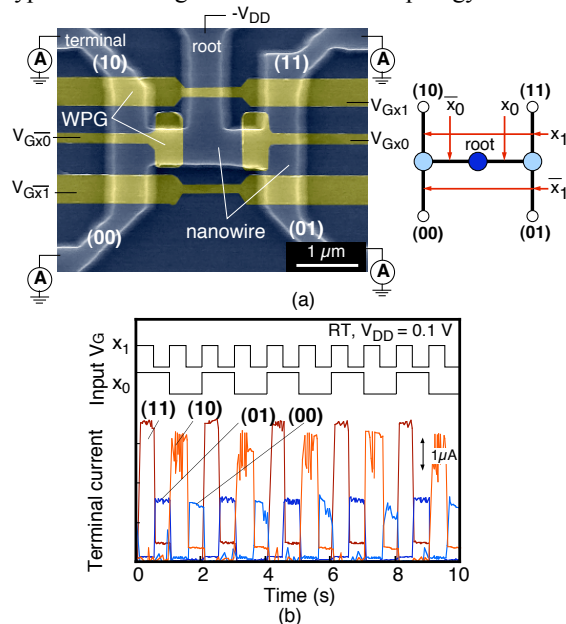


Fig.2 (a) SEM image of the fabricated 2D hypercube with its logic architecture and (b) measured input-output waveforms.

- [1] S. Kasai and H. Hasegawa, IEEE EDL, 23, p.446, 2002.
- [2] S. Kasai, presented at 15th Int. Workshop on Post-Binary ULSI Systems, Singapore, May 17, 2006.
- [3] V. P. Shmerko and S. N. Yanushkevich, Artificial Intelligence Rev., 20, p.473, 2003.