

Hybrid CMOS/Nanoelectronic Circuits

Konstantin K. Likharev*

Stony Brook University, Stony Brook, NY 11794-3800

I will review recent work on devices, circuits and architectures for possible hybrid semiconductor /nanodevice integrated circuits based on nanowire crossbars, with similar, simple, two-terminal devices (with the functionality of programmable diodes) formed at each crosspoint. Special attention will be given to the so-called “CMOL” variety of the hybrids, in which the crossbar is connected to the underlying CMOS circuit with an area-distributed, pin-based interface [1-6]. Such interface allows the CMOS subsystem to address each and every of the crosspoint devices, even with no nanoscale alignment between the CMOS and crossbar subsystems. Detailed studies have shown CMOL may enable (at least) the following applications:

- (i) terabit-scale memories with access time below 100 ns and defect tolerance up to 10% [7],
- (ii) FPGA-like reconfigurable logic circuits with the area-by-delay product at least two orders of magnitude lower than that of CMOS FPGAs fabricated with similar design rules and power per unit area [8, 9], and
- (iii) mixed-signal neuromorphic networks (“CrossNets”) [10] which may provide unparalleled performance for some important information processing tasks including pattern classification [11], global reinforcement with delayed reward [12], and in future may become the first hardware basis for challenging the mammal cerebral cortex in both density and speed, at manageable power.

Recently, the hybrid circuit concept has received a strong boost from the announcement of reproducible fabrication of the necessary crosspoint devices (programmable diodes) based on amorphous silicon and several demonstrations of nanowire crossbars with 15-nm-scale half-pitch.

The work has been supported by AFOSR, DoD, FCRP via FENA Center, and NSF.

1. K. K. Likharev *et al.*, *Ann. NY Acad. Sci.* **1006**, 146 (2003).
2. K. K. Likharev and D. B. Strukov, in: *Introducing Molecular Electronics*, Springer, Berlin, 2005, pp. 447-477.
3. G. Snider and R. S. Williams, *Nanotechnology* **18**, 035204 (2007).
4. D. Tu *et al.*, *Micro & Nano Letters* **2**, 40 (2007).
5. K. K. Likharev, *J. Vac. Sci. Technol. B* **26**, 6 (2007).
6. K. K. Likharev, *J. Nanoel. & Optoe.* **3**, 203 (2008).
7. D. B. Strukov and K. K. Likharev, *J. of Nanoscience and Nanotechnology* **7**, 151 (2007).
8. D. B. Strukov and K. K. Likharev, *Nanotechnology* **16**, 888 (2005).
9. D. B. Strukov and K. K. Likharev, in: *Proc. FPGA'06*, 131 (2006).
10. Ö. Türel *et al.*, *Int. J. of Circ. Theor. Appl.* **32**, 277 (2004).
11. J. H. Lee and K. K. Likharev, *Lecture Notes in Computer Science* **3512**, 446 (2005).
12. X. Ma and K. K. Likharev, *IEEE Trans. on Neural Networks* **18**, 573 (2007).

* E-mail: klicharev@notes.cc.sunysb.edu