Fabrication of titanium oxide tunnel barriers for vertical metal oxide tunneling transistor (VMOTT)

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The scaling down of metal-oxide superconductor field effect transistor (MOSFET) is approaching its fundamental limits due to quantum mechanical and short channel effects. Here we propose a new nano-device, the vertical metal oxide tunneling transistor (VMOTT) which is a modified version of the metal oxide tunneling transistor (MOTT). The main advantages of MOTTs are scalability to nano-scale, high speed, simple fabrication process and elimination of short channel effects. The proposed VMOTT will provide a better design by optimizing the barrier height and the quality of the tunnel oxide. The fabrication of VMOTT can take advantage of the better control on material growth and device processing along the vertical dimension. We chose titanium oxide (TiO_2) as the tunnel barrier, and optimized its growth conditions on p-type silicon (Si) as the first steps towards making a VMOTT operable at room temperature (RT). TiO_2 is a suitable candidate for the tunnel barrier because it is reported to have a low barrier height of about 0.1÷0.6eV depending on the fabrication process. We deposited 10 nm thick Ti layers by vacuum e-beam evaporation on p-type Si (resistivity of 0.02 Ω-cm) without any substrate heating. The wafers were RCA cleaned and HF treated before evaporation. The samples were split into three groups for thermal oxidation at 300°C, 400°C and 500°C for 30 minutes. Samples 1, 2 and 3 were annealed after oxidation in dry N_2 at 700°C for 30 minutes. A 1 μm thick top Al electrode was vacuum evaporated using a shadow mask to make various contact pad sizes and a 1 μm Al layer was evaporated on the back surface. Finally, the samples were heated in N_2 at 450°C for 30 minutes to make the ohmic contacts. The oxide thickness was measured by ellipsometry with laser light at 632.8 nm and an incident angle of 70°. This was verified by cross-sectional scanning electron microscopy (SEM). The oxide thickness and the dielectric constant were determined by analyzing the current-voltage (IV) and capacitance-voltage (CV) data of the metal-oxide semiconductor (MOS) capacitors. Current transport mechanisms in the oxide were identified from the IV data. The TiO_2 tunnel barrier of the VMOTT is fabricated by thermal oxidation of vacuum evaporated Ti at three different temperatures: 300°C, 400°C and 500°C. For samples grown at oxidation temperatures below 500°C, there is a huge leakage current due to the poor quality of the oxide layers. Annealing the samples in N_2 ambient at 700°C reduces the leakage current dramatically by introducing an interfacial SiO_2 layer of about 1 nm thickness. For samples grown at 500°C, there is no significant SiO_2 sub-layer and FN (Fowler-Nordheim) tunneling has been observed at room temperature. The Al/TiO_2 barrier height is determined to be about 0.15 eV with dielectric constant of 67. The main leakage current is contributed by the electrically active defects with barrier height of 0.12 eV in the oxide.

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