

# Contact scaling for advanced CMOS

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Complimentary metal-oxide semiconductor (CMOS) scaling into the nanometer regime brings many challenges for both front-end-of-the-line (FEOL) as well as back-end-of-the-line (BEOL) technology. As it clearly states in the International Technology Roadmap for Semiconductor (ITRS) *we have entered the era of material limited device scaling*, as materials have been pushed to their fundamental limits. Therefore the continued scaling will require the introduction of new tools, and materials, as well as new unit and integrated processes starting with the silicon wafer substrate and extending through contact silicidation processes to advanced interconnect solutions.

Related to the scaling of the gate length, a main thrust of our research & development efforts focuses on attaining progressively shallower junction depths needed for control of short-channel effects, and optimization of silicon-on-insulator (SOI) based CMOS technology providing junction capacitance reduction and lack of body effect. However introduction of SOI substrates and the presence of very shallow, highly doped source/drain regions considerably limit the amount of silicon that can be consumed resulting in scaling of the contact area and contact silicide thickness. The latter relates to the fact that in order to avoid contact leakage, no more than half the contact depth can be consumed in the formation of the silicide. As the critical dimensions are reduced this trend will potentially lead to an increased parasitic resistance as the roughening of the silicide will start to negatively affect device characteristics and at some point the silicide may become discontinuous and therefore not adequately shunt the contact. In addition, because of the lateral scaling of the contact area, the silicon/silicide contact resistivity becomes an increasing component of the source/drain parasitic resistance. Finally, introduction of high-k gate dielectric materials and metal gates may limit the thermal budget and significantly impact the options for contact formation and shunting strategies and further dictate the choice of materials and processes allowed for interconnecting structures.

Therefore we evaluate new materials and processes for producing the contact as well as the self-aligned silicide contact shunt. We investigate how the phase formation kinetics in these ever-smaller dimensions affect the final film morphology of the silicides and how we can reduce the interface roughness to minimize junction leakage. We also aim to optimize the interface between the silicide and the doped contact silicon to minimize the parasitic resistance. The goal is to define the scaling limits of electrically-testable structures with reliable contact vias filled with low resistivity, CMOS-compatible materials and providing good contact to the underlying silicide. In short we describe our attempts to understand the intricacies of formation of reliable contacts for future CMOS structures.

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