

# Femto Joule switching: Review of low energy approaches for the nano era

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Advancement in silicon processing technology has led to miniaturization of devices, power supply voltage scaling, faster transistor switching speeds just to name a few. Along with these improvements are issues such as threshold voltage scaling and interconnect delays. Device miniaturization has also seen a rise of battery operated electronic devices with very stringent energy requirements. Power dissipation thus becomes a major design challenge in highly integrated systems. Leakage currents become significant as the power supply and threshold voltages are scaled. Interconnects also contribute significantly to power dissipation. Low energy techniques are thus very critical.

In this paper we present a review of very low energy design techniques that hold a lot of promise in the nano-electronics era. We also examine the classical low power approaches which include: differential complimentary metal-oxide semiconductor (CMOS) logic, asynchronous methodology, charge recycling and clock gating. We show how some of these techniques will not be sufficient for energy requirements of the nano-era. A comparison of differential CMOS logic gates is presented in and energy computations provided. Perhaps the most energy efficient design approach using differential logic circuits is that of Fahim and Elmasry. The authors basically note that the differential logic family gates are suitable for high performance systems and dissipate considerable power. To reconcile the conflicting high performance and low power issues they employ short circuit currents of CMOS inverters to provide the required switching pulses for their operations and thus lower the energy tremendously. This is managed without sacrificing performance. Another solution is charge recycling which has become an added feature on differential logic gates and is aimed at maintaining the performance gains while reducing power dissipation. In some cases this technique has been coupled with the asynchronous methodology. We show how this charge recycling technique as a low energy technique has some shortfalls.

Efforts to have low energy systems have also seen considerable work at transistor level with researchers seeking to adaptively control the body bias, performing operations with power supply voltages lower than the threshold voltages, and using leakage currents to drive the operations. Finally, efforts on low power emerging devices are mentioned in the 2003 ITRS (international roadmap for semiconductors) section on *Emerging Research Devices*. In ITRS-Table 63a the projected parameters for logic single-electron tunneling (SET) devices are: 40 nm (spatial pitch), 1 GHz (switching speed), 1 aJ (switching energy), at an operational temperature of 20K. Recently, a capacitive SET 16-bit threshold logic adder was presented. It has 104 gates (208 SET devices), runs at 500 MHz with a switching activity of 30%, while dissipating less than 11 pW. Putting all this numbers together, it follows that for this particular design the average switching energy of one SET device is:  $11 \text{ pW} / 500 \text{ MHz} / (30\% \text{ switching activity} * 208 \text{ devices}) = 0.00035 \text{ aJ}$  at helium temperatures, growing up to 0.3 aJ per SET at 20K (smaller size SET devices could run room temperature).

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