# High-k gate stack interface properties and device performance

G. Bersuker *, J. Sim, C. Young, B.H. Lee, J. Barnett, N. Moumen, B. Foran, P. Lysaght, P. M. Zeitzoff, H. R. Huff

*International SEMATECH, Austin, TX, USA.*

To sustain the historical rate of interconnect performance growth, future generations of transistor technology may require using gate dielectric materials with higher dielectric constant k than k = 3.9 of conventional silicon dioxide. The class of materials exhibiting high k values consists of transition metal oxides, which inherently possess a high density of structural defects. These defects, typically representing fixed charges and electron traps, adversely affect device characteristics. However, effects caused by these defects can be modulated by an additional factor of significant importance; that is the presence of the interfacial thin $SiO_2$-like layer between the high-k film and the Si substrate. This interfacial layer can be formed during high-k film deposition since an excess of oxygen in the MOCVD (metal organic chemical vapor deposition) process or the $H_2O$ cycles in the ALD (atomic layer deposition) process are utilized to minimize the formation of the oxygen vacancies. In this study, we evaluate the interface properties of the high-k gate stacks and discuss the contribution of the interfacial layer to the critical transistor parameters. Oxygen diffusion in the high-k films is usually higher than in $SiO_2$ and, therefore, the bottom portion of the interfacial layer may be expected to be oxygen deficient. This reduced oxygen content leads to a reduction of the energy band gap and, hence, lowers the effective band offset and dielectric strength of the interfacial layer with respect to the bulk $SiO_2$ value. Physical properties of the interfacial layer are found to correlate to the channel carrier mobility. Stress-induced degradation of this interfacial $SiO_2$-like layer, whose properties are also strongly dependant on the pre-high-k deposition treatment, may be primarily responsible for the stress-induced high-k gate stack degradation observed under certain operating conditions.

* Corresponding author. Tel. 512-356-7045.
*Email address:* gennadi.bersuker@sematech.org (G. Bersuker).