

# Fully silicided (FUSI) gate devices as a *metal* gate option for advanced CMOS

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As ULSI (ultra low-scale integration) dimensions continue to shrink at a phenomenal pace, novel materials are required for deep sub-micron high-performance devices. This is especially true for gate dielectric, the heart of MOSFETs (metal oxide semiconductor field effect transistors). The equivalent thickness of the gate dielectric is already on the order of 2 nm (and thinner) and is projected to be close to 1 nm soon. Direct tunneling currents, reliability, boron penetration from poly-Si gate, mobility degradation, and other fundamental issues are of a serious concern for such ultrathin oxides. Besides, poly-Si depletion causes parasitic series capacitance that is equivalent of approximately 0.4 – 0.5 nm of electrical thickness of gate oxide and can not be ignored for sub-2 nm gate stacks. One way to overcome the poly-depletion problem is to use metal gate electrodes instead of conventional poly-Si gate materials. Another promising approach is to fully silicide poly-Si gate. In this way, gate electrode shows a metal-like behavior and is easier to integrate with conventional silicon technology.

In the presentation, we will discuss material and electrical characterization of FUSI gates, as well as integration issues. We will show that FUSI gates offer approximately 0.5 nm reduction of electrical thickness in inversion ( $T_{inv}$ ) for a given gate stack compared to conventional poly-Si gate electrode. Workfunction control, an important issue for high-performance CMOS (complimentary metal oxide semiconductor) devices, will also be addressed. Aggressive scaling below 2 nm dictates the use of high-k insulators. Results on FUSI technology on high-k dielectrics and issues associated with it will be presented. Finally, we will discuss an important aspect of reliability of FUSI gates and compare to current poly-Si/SiO<sub>x</sub>N<sub>y</sub> technologies.

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